AMENDMENTS TO THE SPECIFICATION

Please amend paragraph #0060 as follows:

--The host device (scheduler) 28 is generally a timing mechanism for scheduling and enabling activation of the devices in system 10a. An exemplary scheduler 28 for enabling the scheduling and synchronization of operations and data transfers intended to be performed by particular devices 12a, 14a at specific predetermined times in an operational cycle is disclosed in commonly-assigned copending U.S. Patent Application No. ~~09/xxx,xxx, Attorney Docket No. 22682-06281~~ 10/033,857, filed November 2, 2001, entitled "Video Processing Control and Scheduling", ~~by Sha Li, *et al.*,~~ the subject matter of which is herein incorporated by reference it its entirety.--

Please amend paragraph #0064 as follows:

-- Multi-channel data bus controller 30a ("controller 30a") is enabled to receive address information (ctrl_addr) 50 from the control bus 18, and is capable of sending data and receiving data (ctrl_data) 52 respectively to and from the data bus 20. Additionally, controller 30a is communicatively coupled to the control bus 18 to receive data enable signals 53, 54, 55 (e.g., read 53, write enable 54, Address Latch Enable (ALE) 55, referred to as ctrl_rd/we/ale for convenience), an input output ready (ctrl_io_ready) signal 56, direct memory access request (Dma_req(s)) signals 58, transfer ok (transfer_ok) 60 signals, and an interrupt direct memory access (int_dma) signal 62. Controller 30a receives scheduler command signals 64 broadcasted from the scheduler 28 over command bus 22, as described in more detail in U.S. Application No. ~~09/xxx,xxx, Attorney Docket No. 22682-06281~~ 10/033,857, filed November 2, 2001, the subject matter of which is incorporated by reference herein.—

Please amend paragraph #0126 as follows:

--Both the READ and WRITE cycles are preferably uninterruptible, and after these operations, the data in the output data register is already written to the client device. The input data register holds the data read from the client device. Because after a READ cycle 304, the controller 26 may be interrupted before it uses the data in the input data register, the interruption service should preferably save (e.g., push) the input data register, and restore it upon return from the interrupt. Further details about the operation of BIU 27a are described in U.S. Application

No. ~~09/xxx,xxx, Attorney Docket No. 22682-06281~~ 10/033,857, filed November 2, 2001, the subject matter of which is incorporated by reference herein.--

Please amend paragraph #0127 as follows:

--FIG. 15 illustrates an exemplary implementation of a BIU 40a, that is a part of the multi-channel data transfer controller 30a and the devices 38. BIU 40a generally functions as the client BIU communicatively coupled to the host BIU 27a. BIU 40a includes an address & WR/RD# buffer 370, a state machine 372, a input buffer 374, and output buffer 376, and a tristate latch enable buffer 378. The operation of BIU 40a is described in more detail in U.S. Application No. ~~09/xxx,xxx, Attorney Docket No. 22682-06281~~ 10/033,857, filed November 2, 2001, the subject matter of which is incorporated by reference herein.—

Please amend paragraph #0129 as follows:

-- To start the data transfer by hard-wired request, the scheduler 28 preferably provides the number of the configuration to the scheduling bus 22 with an asserted schedule command valid signal. FIG. 16 illustrates a signal flow diagram and chart detailing the operation of how a channel is established in accordance with one aspect of the present invention. In order for a device 38 to access the memory device 34 in either a READ or WRITE data transfer, the scheduler 28 broadcasts a schedule command 64a and a valid command 64b as described in detail in U.S. Application No. ~~09/xxx,xxx, Attorney Docket No. 22682-06281~~ 10/033,857, filed November 2, 2001, the subject matter of which is incorporated by reference herein. These commands 64a, 64b indicate a start of channel 1, by way of example. In response, the controller 30a loads 380 the channel configuration data into the configuration register file 44a. Also, the requesting device 38 preloads 382 and initializes either a READ or WRITE request command for memory device 36. The device sends 384 a W/R transfer request 58 to controller 30a, which in turn parses request 58 into a wreq 66 or a rreq 68 as seen in FIG. 4. Once the controller 30a receives 386 the W/R request, the configuration register file is accessed to activate 388 the channel for the data transfer, and the data transfer is undertaken 390. After the last_transfer signal 72 is received by the controller from the device 38, the controller 30a sends 392 a transfer_ok signal 74 to the device 38. It is noted that the transfer_ok signal 74 can be used to

indicate the completion of data read from a memory device to another device, or of data written to a memory device, by way of example. The controller 30a then transmits 394 a control command to the memory controller 34.--

Please amend paragraph #0132 as follows:

-- FIG. 18 is a timing diagram of a READ transfer being initiated. The Start_dma signal represents the schedule command signal and the DMA configuration (DMA_conf) signal represents the schedule valid signal broadcast by the scheduler 26 as described in U.S. Application No. ~~09/xxx,xxx, Attorney Docket No. 22682-06281~~ 10/033,857, filed November 2, 2001, the subject matter of which is incorporated by reference herein. The valid_xfr_rd signal is generated by the controller 30a for a READ transfer, and when active, there should be valid data read from the memory device 36 to the data bus 20.--